Energy Consumption of Array-Based Logic Gates

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Abstract

Array based transistor stacking has been shown to be an effective technique for improving the power and delay of digital circuits operating in the subthreshold to above nominal voltage range which eventually gives an advantage in overall power-delay-product (PDP) and it comes at the cost of power consumption and area. However, our observation shows that using array based approach, nor all logic cells neither every technology gives an improvement in energy consumption. In this paper, we present our observations to identify whether using array based transistors is beneficial (or not) in comparison with conventional approach in 150 nm technology. The results of incorporating the array-based methodology in standard logic gates such as INV, NOR3 and NAND3, using 150 nm technology, shows that there is not as such improvement by using array-based approach in term of Energy consumption (PDP).

Keywords: *CMOS, Subthreshold region, Low power, power-delay-product (PDP), Transistor sizing.*

I. INTRODUCTION

In digital VLSI design configuration space, extensive consideration has been given to the strategy of high performance chips. The expanding consideration on power consumption and delay in circuit configuration has encouraged a noteworthy investigation for optimal power for a given execution. In certain rising applications, for example, small scale sensors, medical application, control, and power effectiveness concerns conventional emphasis on energy and delays. These systems can be worked at reduced performance execution levels with a specific end goal to extend their battery lifetimes. Numerous such as low performance systems utilize least energy in the near-Vth area, where the power supply voltage is under the device threshold voltage. This motivates the investigation of subthreshold region digital circuit performance and design techniques [1].

This paper mainly focuses on analysis of digital circuits operating in variable voltage supply for observing low power and minimum delays in a typical 150 nm technology. Propagation delay in the digital logic circuits can be attained by placing transistors in parallel with minimum width. The reduction in delays of CMOS brings transistor behavior near to ideal. The array-based approach shown that the minimum power and delay depends on the supply voltage and the implemented array-based logic characteristics methodologies. The Power-Delay Product (PDP) has been compared for conventional and proposed scheme i.e. Array based transistor stack approach with optimum width sizing. It has been exposed that using proposed technique operating at subthreshold to above minimal voltages, substantial PDP savings can be realized in applications demanding low to medium frequency of operation [2], however, this kind of improvement is not valid for any technology. This paper is organized as follows: Section II is about previous related work for PDP. In Section III and IV, we analyze the PDP observation through experimental work. Results and analysis are given in section V, and the last Section VI concludes the paper.

II. RELATED WORK

The optimum widths found for both nmos and pmos transistor types; any circuit designed near-threshold can be enhanced in term of performance by replacing the large, single transistor with array of transistors all sized at the subthreshold minimum width.. This additionally applies for the transistor stacks that show up in gates, for example, NAND and NOR since the subthreshold minimum width has likewise turned out to be best to maximize the current-to-capacitance proportion. Using array based transistor stacks of the optimum width, keeps the current-to-capacitance proportion at its maximum while producing more elevated amounts of current, rather under going to exponential decay [2].

It is obvious that the current and subthreshold voltage of CMOS transistors at a power supply of 0.3 V in a 65 nm low power technology is powered for maximum current drive as the width limits, and the current seems to be higher than would be expected at the narrow widths [2]. Digital circuits working in the threshold area benefit by low-power consumption at the cost of speed and delay. It is demonstrated that using just transistor widths that expand the current-to-capacitance proportion, either independently or in parallel stacks, as suitable, prompts fast circuits behavior [3]. Most recent, designing of digital subthreshold circuits logic was examined with transistors functioned in the region where supply voltage (Vdd) less than the threshold voltage (Vth) of

the transistor. Parallel Transistor Stacks (PTS) has been appeared to be a viable procedure for enhancing the speed of digital circuits operating in the subthreshold region which comes at the cost of power consumption and area [3]. Digital computation using subthreshold has gained a wide interest in recent years to achieve ultra-low-power consumption in portable computing devices. Digital logic circuits have been extensively studied with design consideration at various levels of abstraction in VLSI area of research.

Maitham Shams and Farhad Ramezankhani. [4], demonstrates the ideal of PMOS to NMOS width proportion for efficient subthreshold CMOS circuits. They proposed the utilization of an ideal beta specific to subthreshold operation that out comes in the greatest frequency of task. Changing a MOSFET's width (W) extremely influences its current and limit voltage in the subthreshold area. In this manner, to calculate out the best transistor width to accomplish the maximum speed, they investigate the performance of threshold voltage, current, and capacitance versus the width of the MOSFET in the subthreshold area. Using beta opt in addition to fingers indicates significantly more enhancements regarding the estimation variables [4]. The fundamental idea in [2] and [5] is to break more extensive than least width transistors into different ïn˘A¸ngers, each with the minimum width so as to enhance metric of digital circuits that characterizes speed and energy consumption. Enhancing the execution of these circuits is important to make subthreshold operation feasible in the embedded and high performance applications, for example, baseband and broadband communication network [6]. In [7], a structure for picking the ideal transistor-stack estimating is proposed for a subthreshold design. The effect of the inverse narrow width impact (INWE) on transistor estimating for the subthreshold process was not measured. In [8], the utilization of logical effort in subthreshold circuits is investigated. It is demonstrated that low energy operation is accomplished when power supply is adjusted under the limit voltage that is known as sub- threshold operation [9, 10]. In [11]. Milad Jalalia and Seyyed Reza suggested the improvement in performance in term of power utilization, propagation delay and power delay product (PDP) in examination with the current full adders. It is presented in [12] that designing subthreshold advanced digital circuits utilizing just comparably estimated PMOS and likewise sized NMOS transistors typically results in quicker circuits than those scaled by regular design techniques, for example, Logical Effort.

III. EXPERIMENTAL SETUP

In this paper, our work is observing and analysis of the consumption of power and improvement in delay of digital circuits by using 150 nm technology. The overall consumption in power-delay-product (PDP) can be achieved by using array based approach over conventional design. This experiment work gives proper analysis in PDP by placing transistors in conventional design as well as in parallel (array-based) with optimum width of NMOS and PMOS circuits. The focus of experiments in this paper has covered both approaches i.e. Conventional and array based on standard logic gates such as INVERTER, NAND and NOR gates. The subthreshold minimum width set up for both transistors NMOS and PMOS, any circuit designed in threshold region can be improved for better performance by replacing the huge, single transistor with array of transistors all widths at the optimum size.

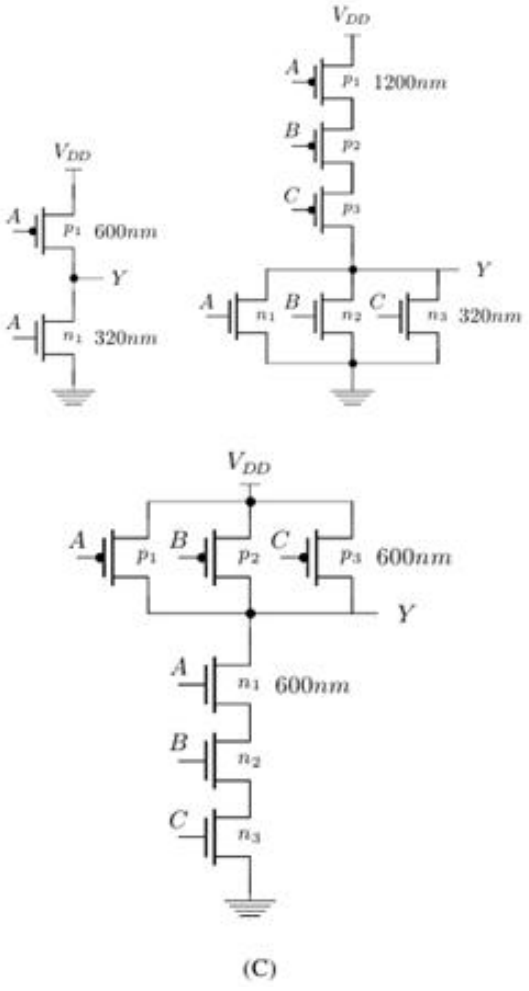

Fig 1: Schematics for Conventional Design: (a) INVERTER; (b) NOR3; and (c) NAND3

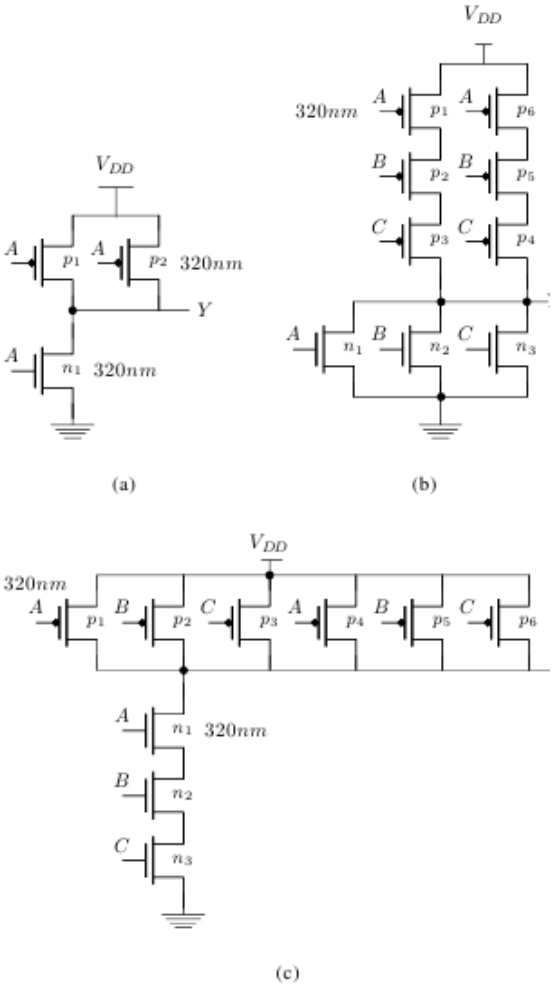

Fig 2: Schematics For Array Based Design: (A) Inverter; (B) Nor3; And (C) Nand3

Fig.2 represents the conventional design of INVERTER, NOR3 and NAND3 with standard width sizes. The operating voltage from subthreshold (0.3) to above minimal voltage (2.0). While looking into array-based design in Fig.2 of three standard logic gates, carries multiple copies of PMOS circuit. All NMOS and PMOS of each logic circuit have optimum width at 320/150 nm. The optimum width can be estimate from current over capacitance ratio where maximum current appears at the most minimal width of transistor. The behavior of circuit depends upon voltage supply and the approach we are using that will reduce energy consumption.

In graphical representation Fig3, Fig4 and Fig5 shows the energy consumption (PDP) curve of both conventional and array based design respectively. It is observed with multiple copies of pmos that there is no as such improvement in energy consumption (PDP) especially in NAND3 gate, however, slighter improvement can be seen in case of INVERTER and NOR3 logic gates.

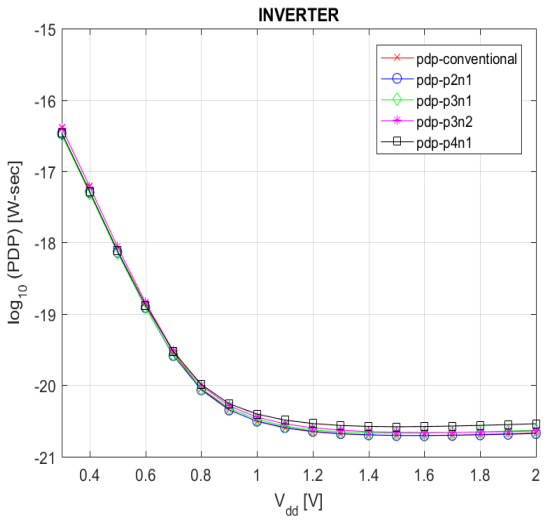

Fig 3: Energy Curve Of Inverter

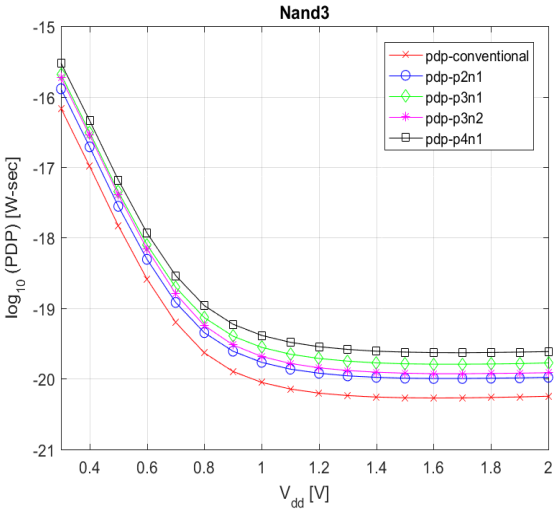

Fig 4: Energy Curve of Nand3

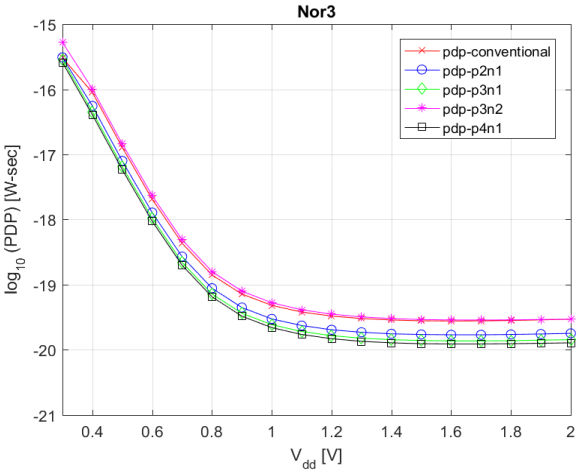

Fig 5: Energy Curve of Nor3

IV. RING OSCILLATOR SIMULATION

Since PMOS COC for LVT transistors keeps increasing with increase in width for a considerable range at the start, as proposed by Nabavi et.al., Wopt for PMOS needs to be found through ring oscillator simulations. The following shows the sim results of a 9-stage inverter based ring-osc, NMOS width is 320nm while PMOS width is swept from 320n to 4um to find the highest frequency for different values of VDD.

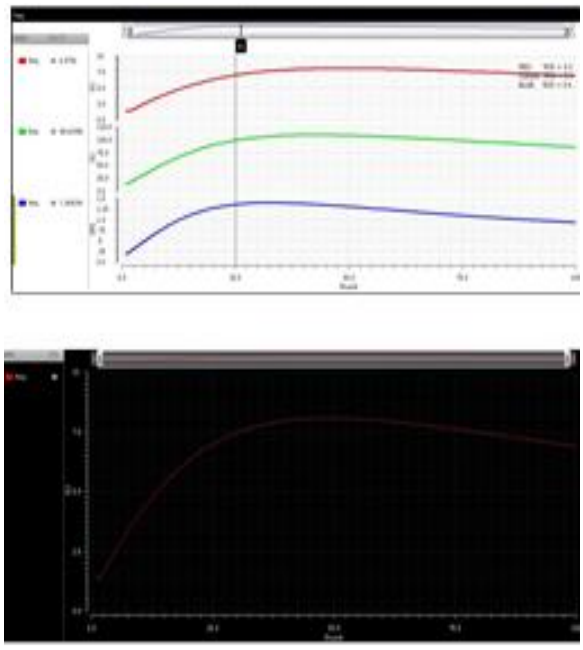

Fig 6: Frequency of 9-stage Ring-Osc. Versus the Width of PMOS

V. RESULTS AND DISCUSSION

We have simulated the standard logic gates spice netlist on spectre cadence simulator [17] to validate our observation for both conventional and array-based design. Although we have not achieved improvement in INVERTER and NAND logic gates. However, significant improvement in energy consumption (PDP) can be seen in NOR gate design with array-based stacking of CMOS cells. To exhibit the adequacy of splitting a large size transistor into array of transistors, an inverter, nor and nand logic gates are simulated between 0.3-2.0 voltage range in 150 nm technology as indicated by the three arrangement shown in figure 1-2. The figures 3-5 have shown the PDP curve at different voltages for both conventional and array-based design. We have used multiple copies here of PMOS such as P2N1, P3N1 and P4N1. . In case of ring oscillator with N stacking of transistors, there is slight boost in term of speed and energy with less delay among all types in Table-1.

Table 1: Optimization in Ring-Osc

TYPE/PARAMETR	FREQUENCY	DUTY CYCLE	INVERTER DELAY	PDP
	(kHz)		(nsec)	(f or 10^-15)
No-PTS	652.2	50.05	85.18	1.034
NPTS	668	50.03	83.17	0.83
PPTS	276.5	49.78	200.9	1.125
NPPTS	280.2	49.72	198.3	1.128

%frequency increase = 2.4
%EDP decrease = 2.13

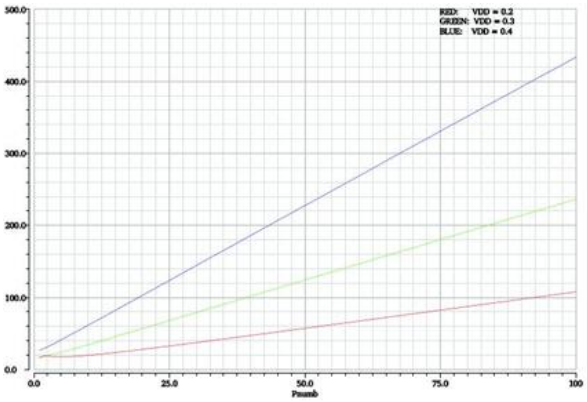

Fig 7: PDP of the 9-stage Ring-Osc. across Width of PMOS and different VDD

Table 1 shows optimization in frequency as well as in energy consumption (PDP). We had examined conventional (no-pts), P stack and N stack of CMOS to form ring oscillators and it provides best combination in NPTS (N stack) with 2.4% improvement in frequency and 2.13% in energy consumption (PDP).

VI. CONCLUSION

All Improving in performance of CMOS circuits while decreasing their power consumption can enlarge the application range of digital circuits. We have demonstrated our observation for both array based design scheme to study the PDP and frequency optimization with significant proportion as compared to conventional design in the subthreshold voltage to above minimal region. The study of analysing array-based scheme is fairly common and appropriate to other standard logic cells. Another prospect of this scheme is to optimize the reliability of circuit in term of Static Noise Margin (SNM) that will give near to ideal response of the circuit.

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